

FIG. 1

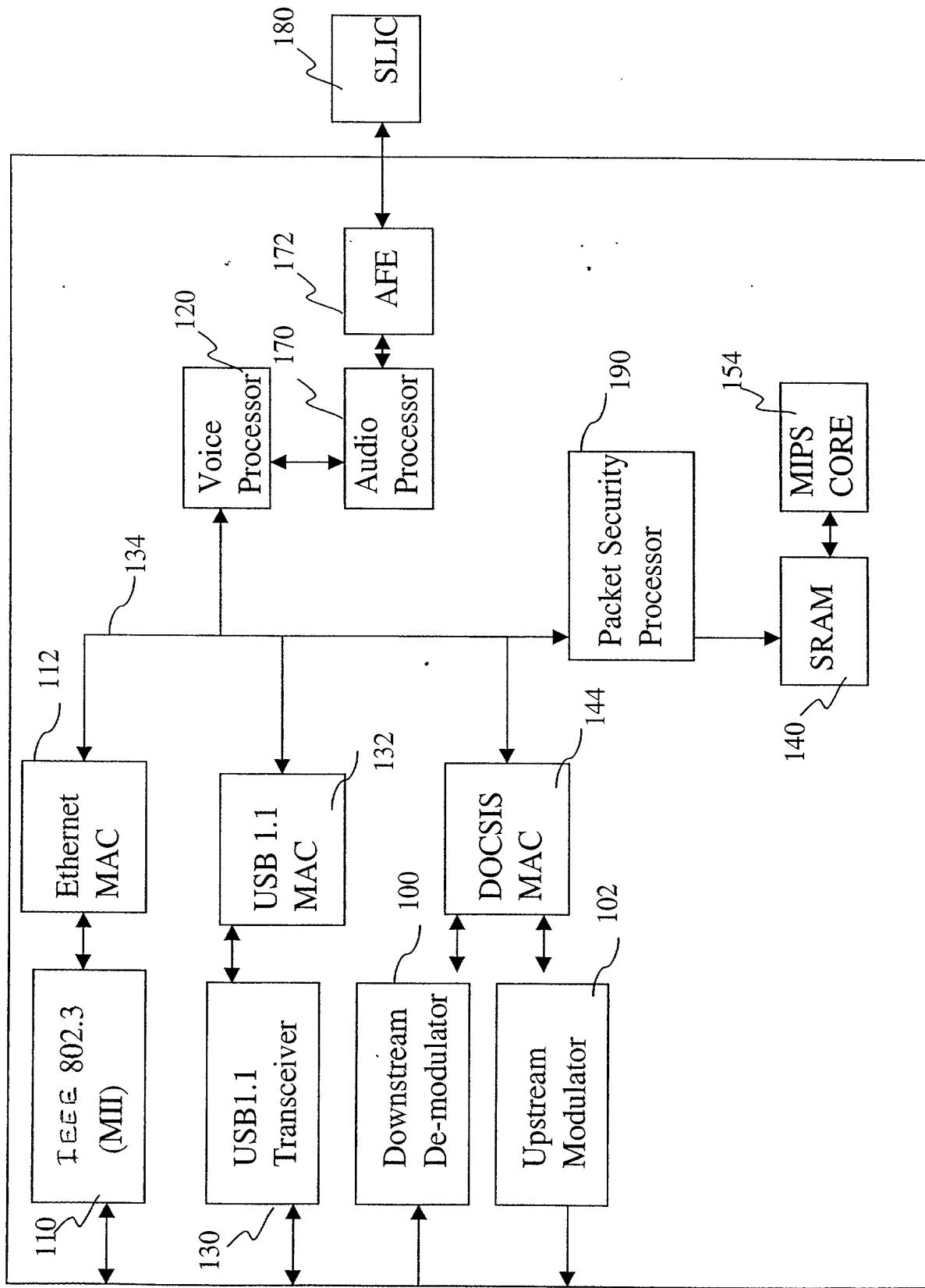


FIG. 2

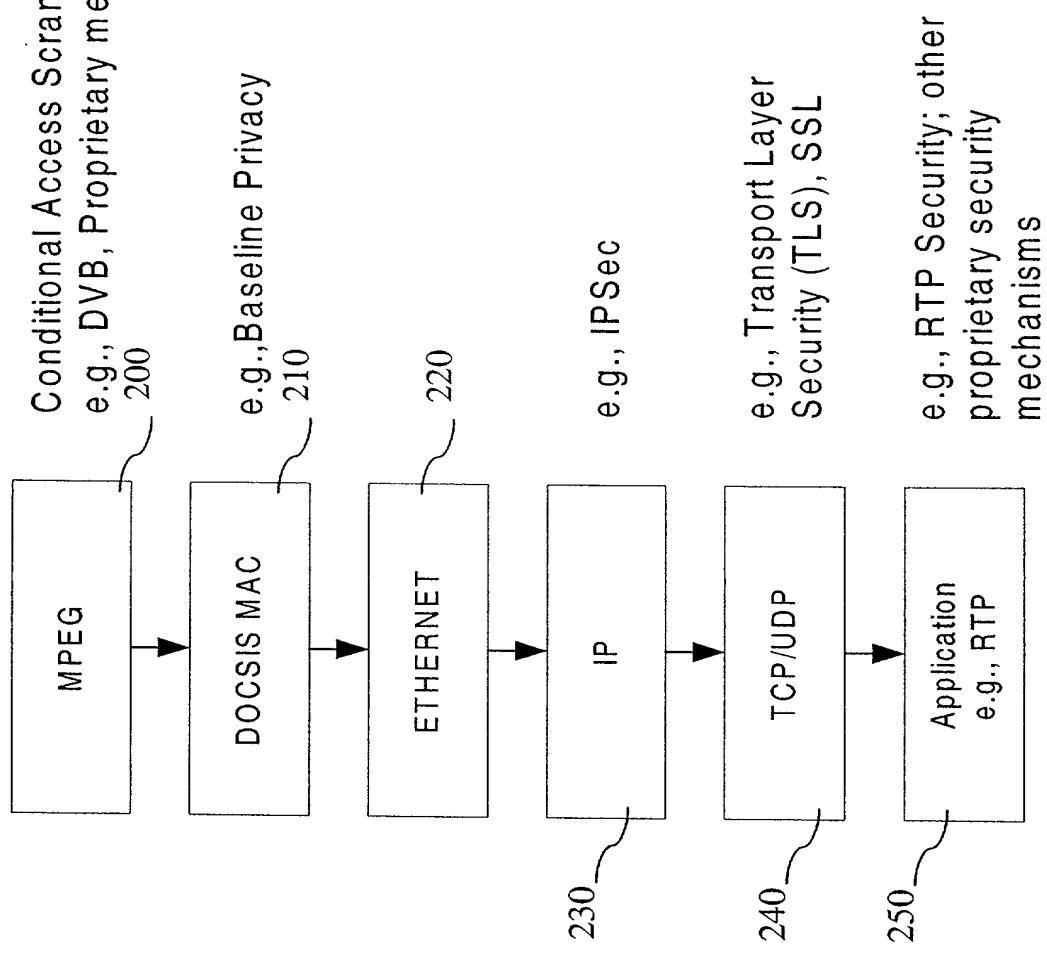


FIG. 3

FIG. 3 illustrates a data processing system architecture. The diagram shows a flow from an external source through an Input Sync block (300) to a PID Parser block (302). The PID Parser block outputs to an Output Buffer (304), which then feeds into a series of four parallel processing blocks: DES (306), 3DES (308), DVB (310), and HMAC (312). Each of these four blocks receives a 4-bit input signal (labeled '4') and has a corresponding 4-bit output signal (also labeled '4'). The outputs of these four blocks converge at a central point, indicated by a downward-pointing arrow, before entering a final Output Buffer (314).

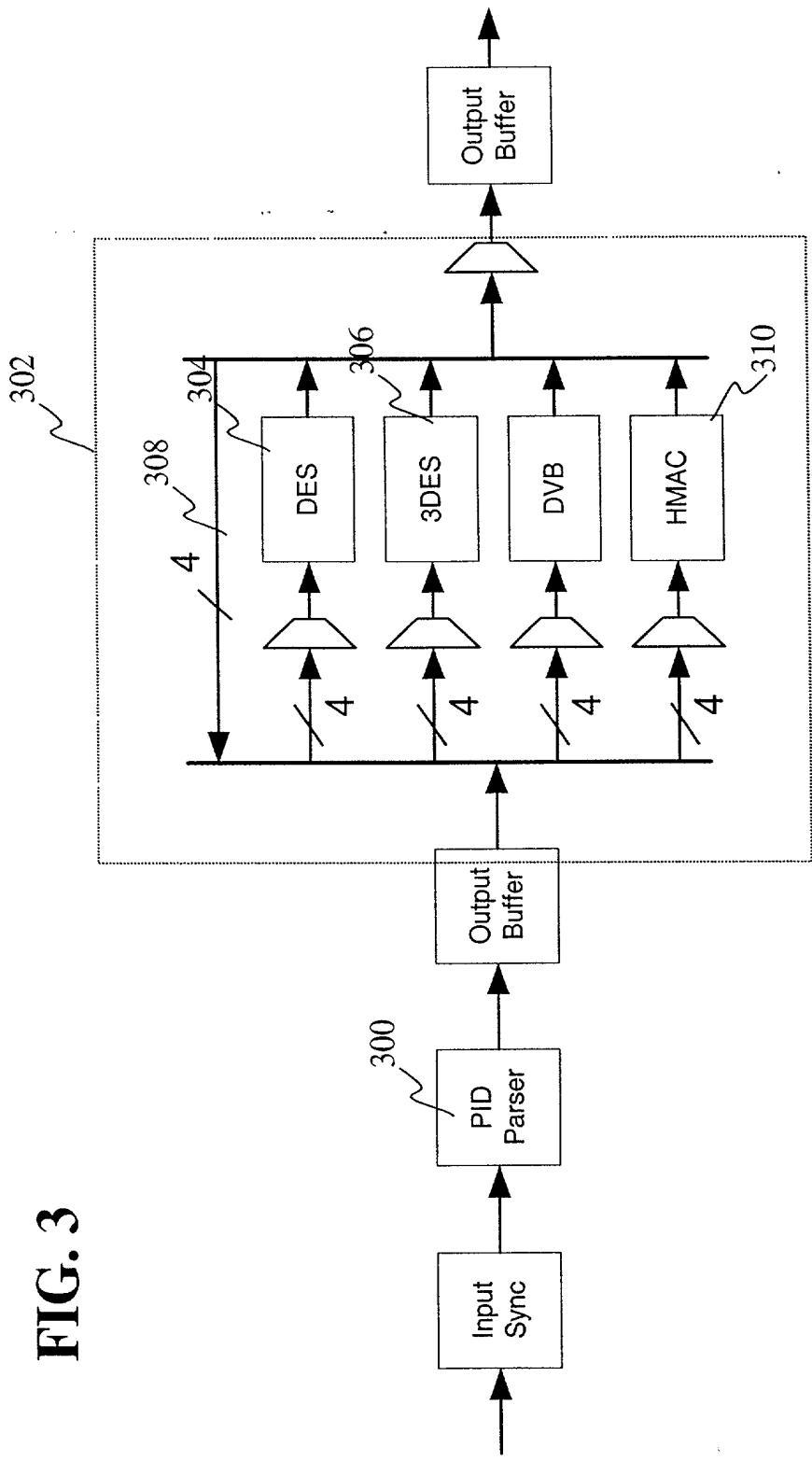


FIG. 4

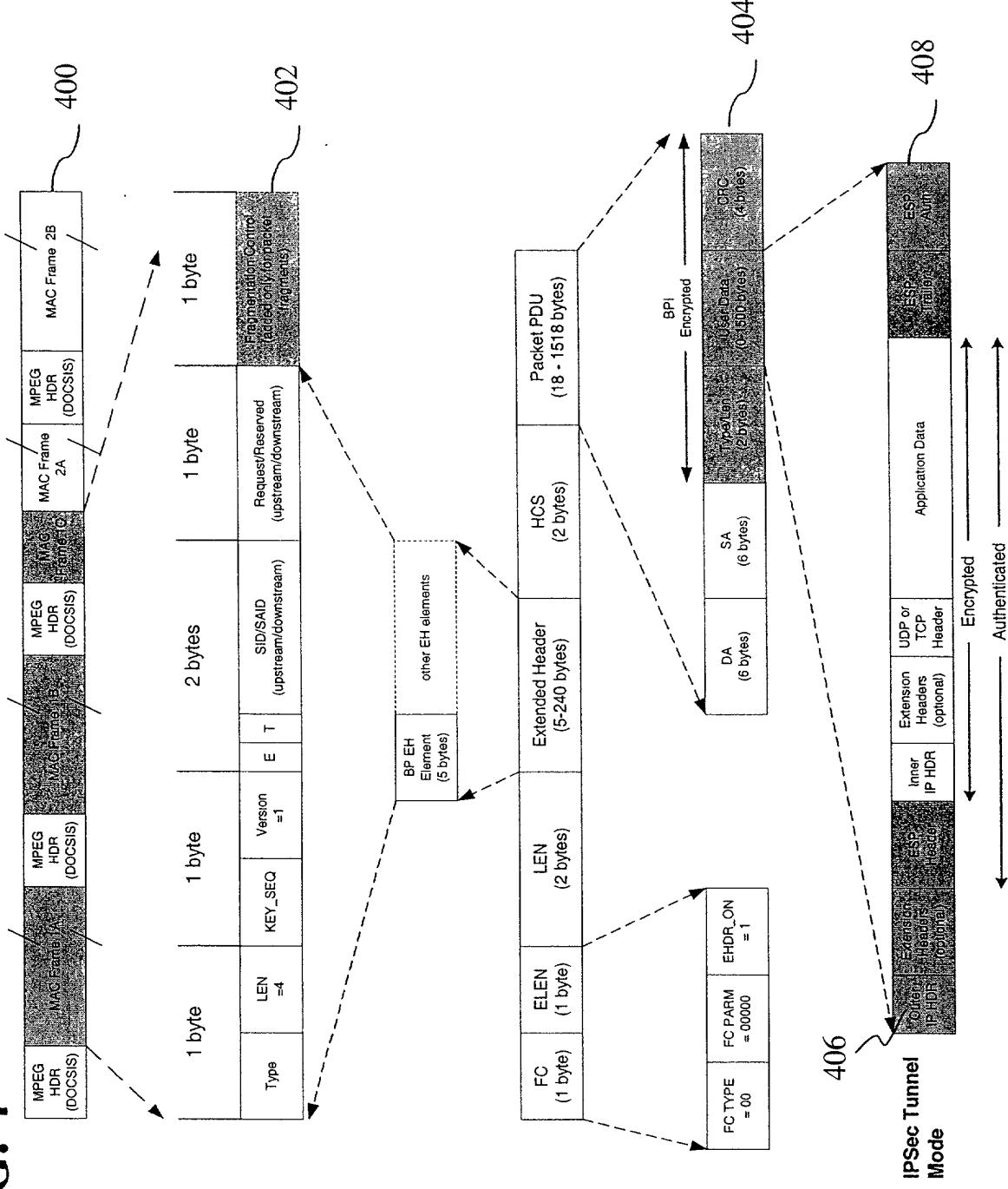


FIG. 5

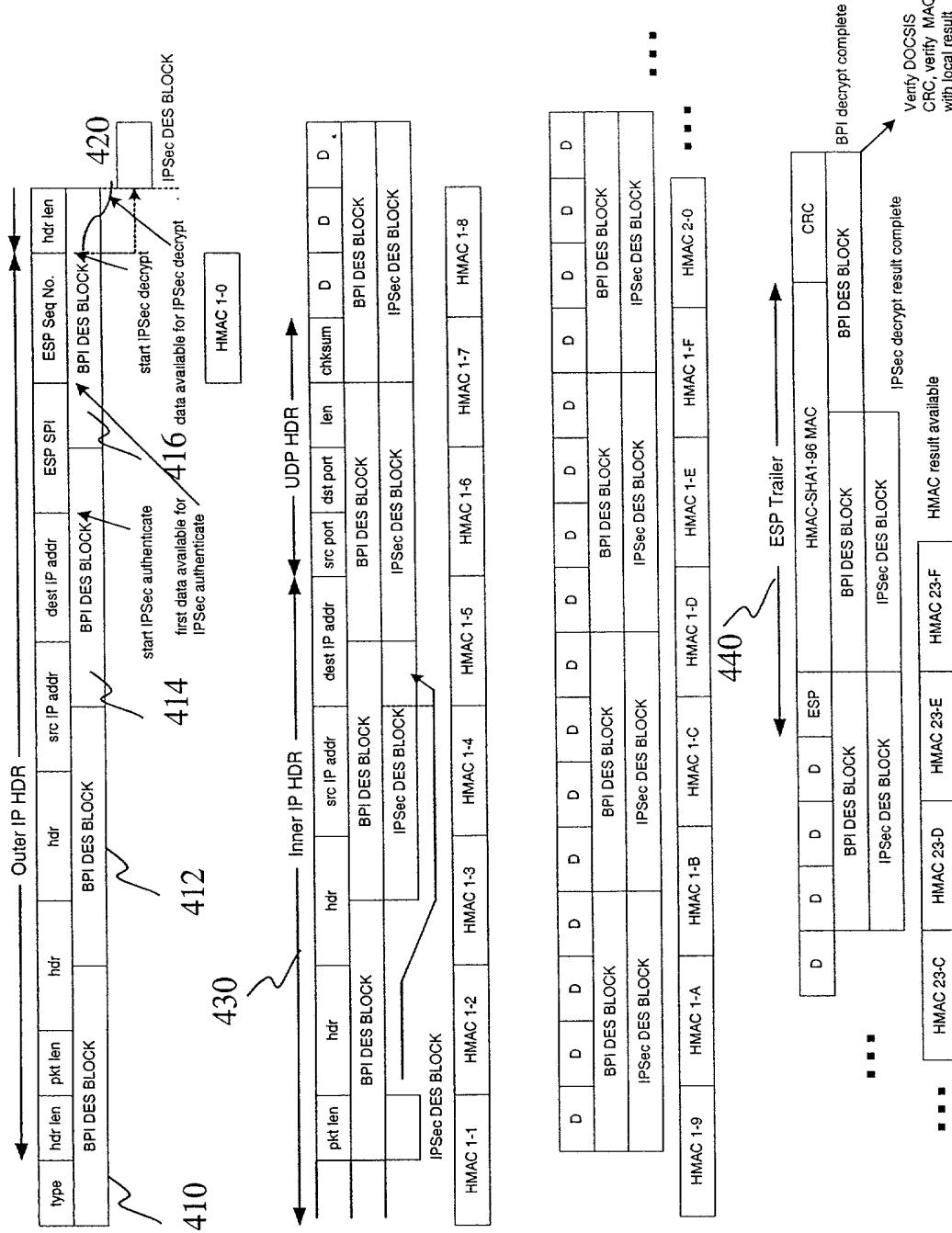


FIG. 6

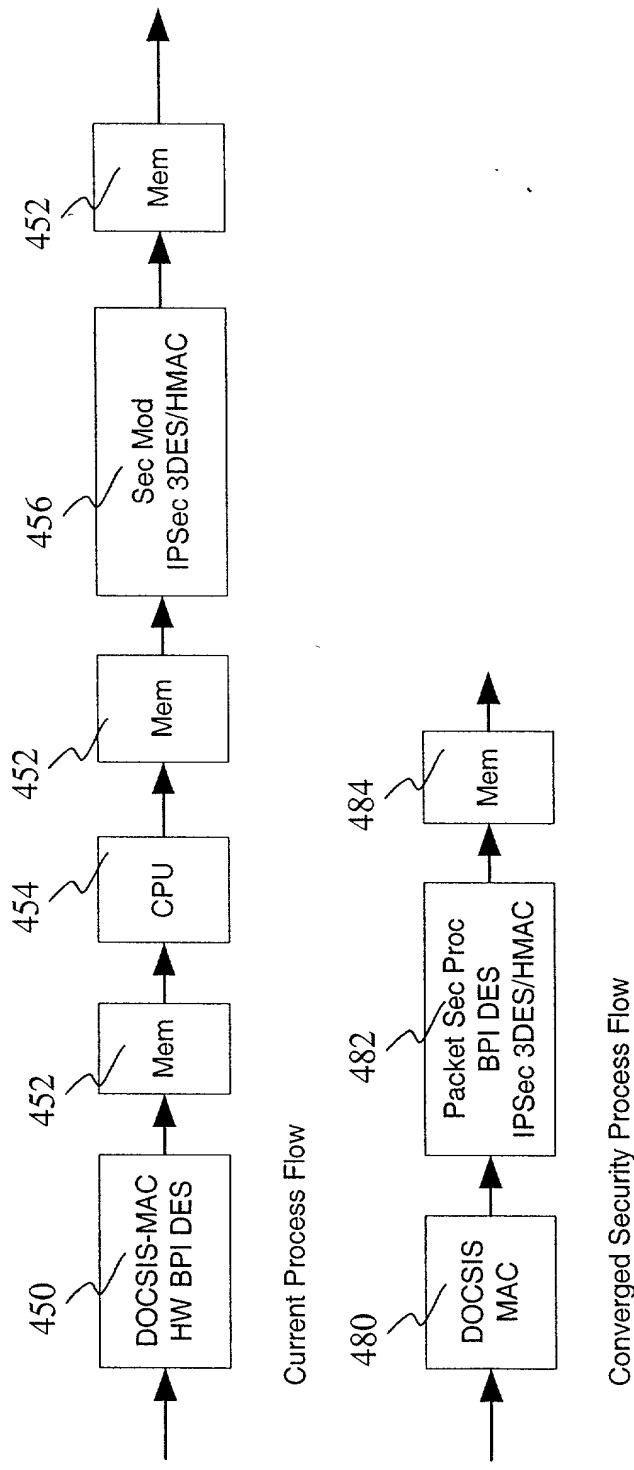
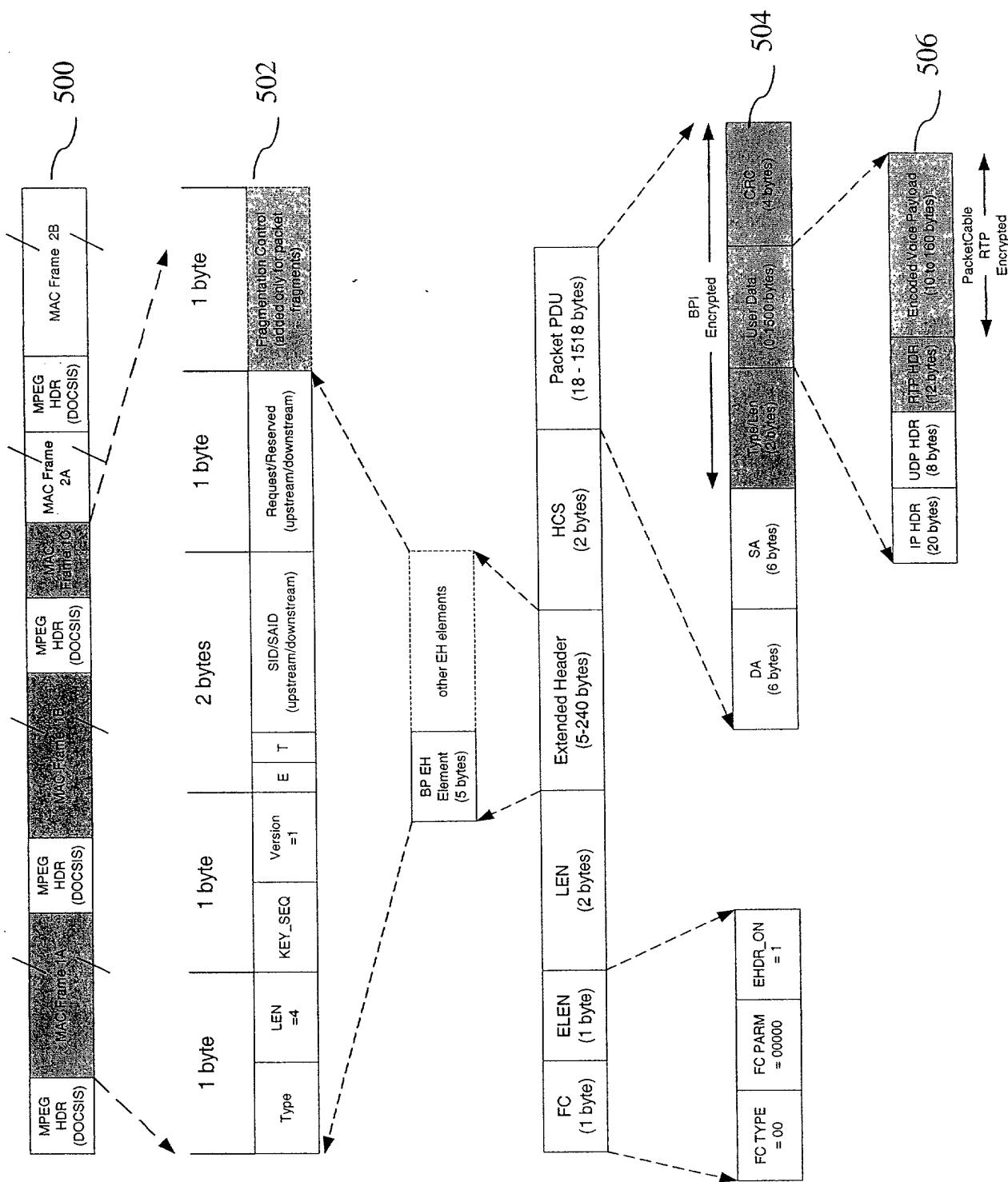


FIG. 7



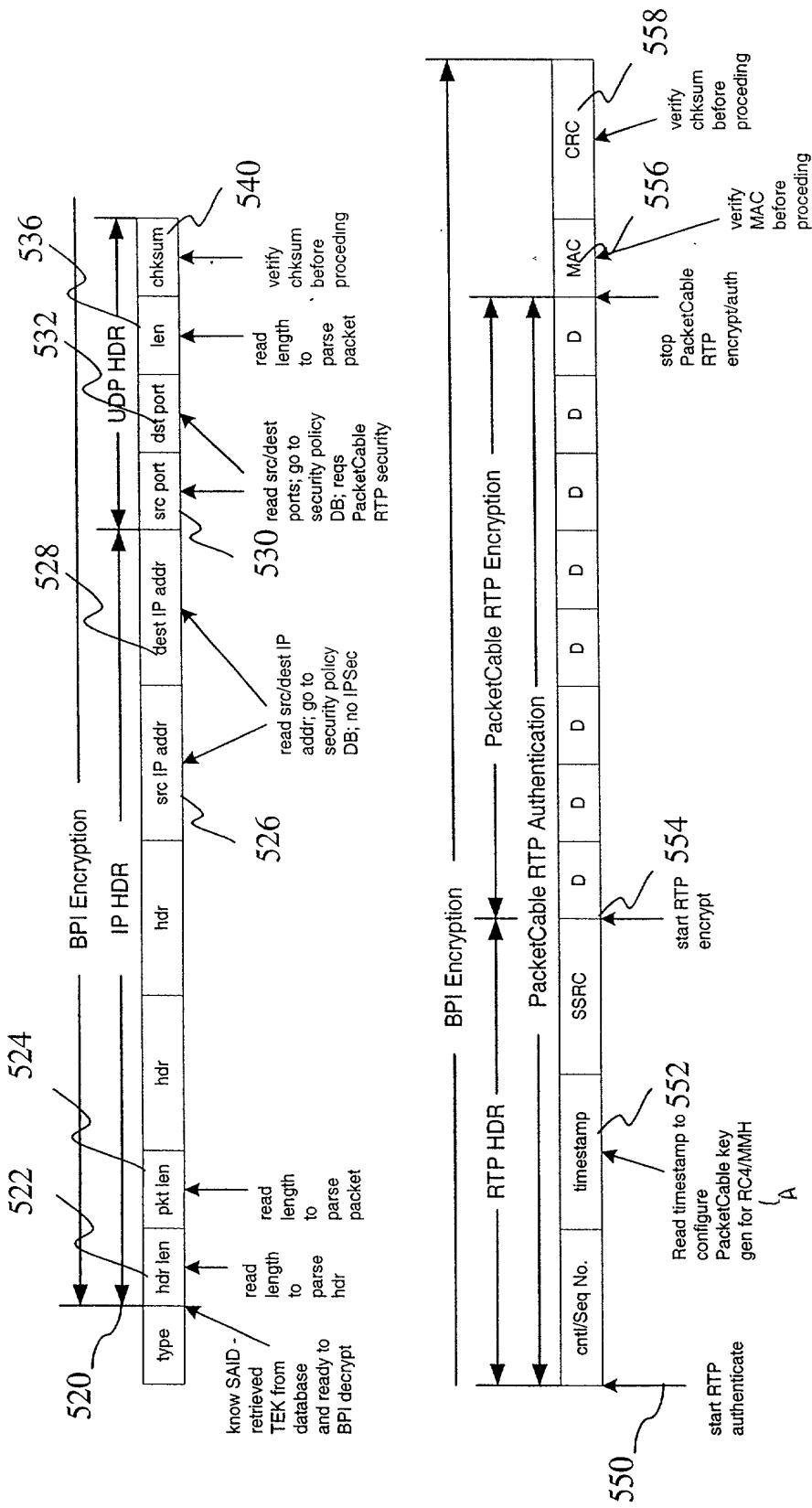


FIG. 8

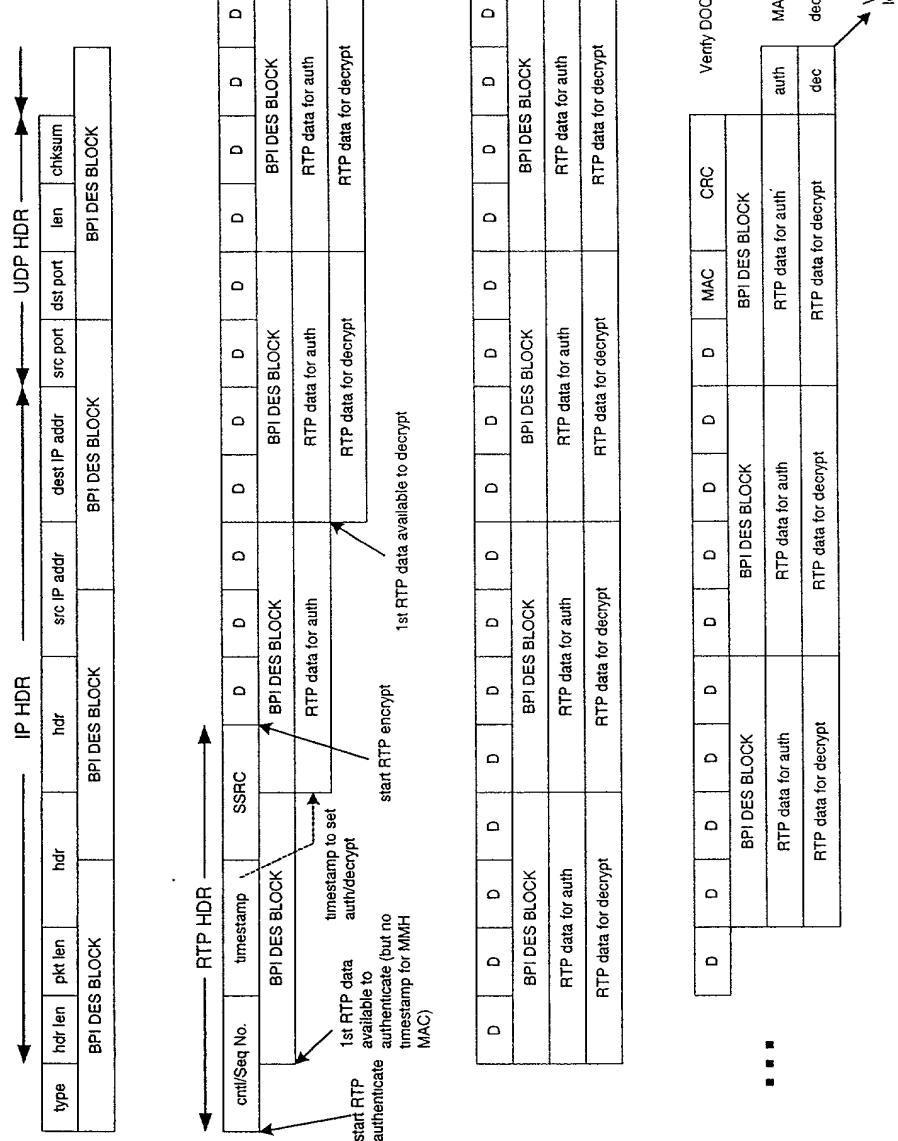


FIG. 9

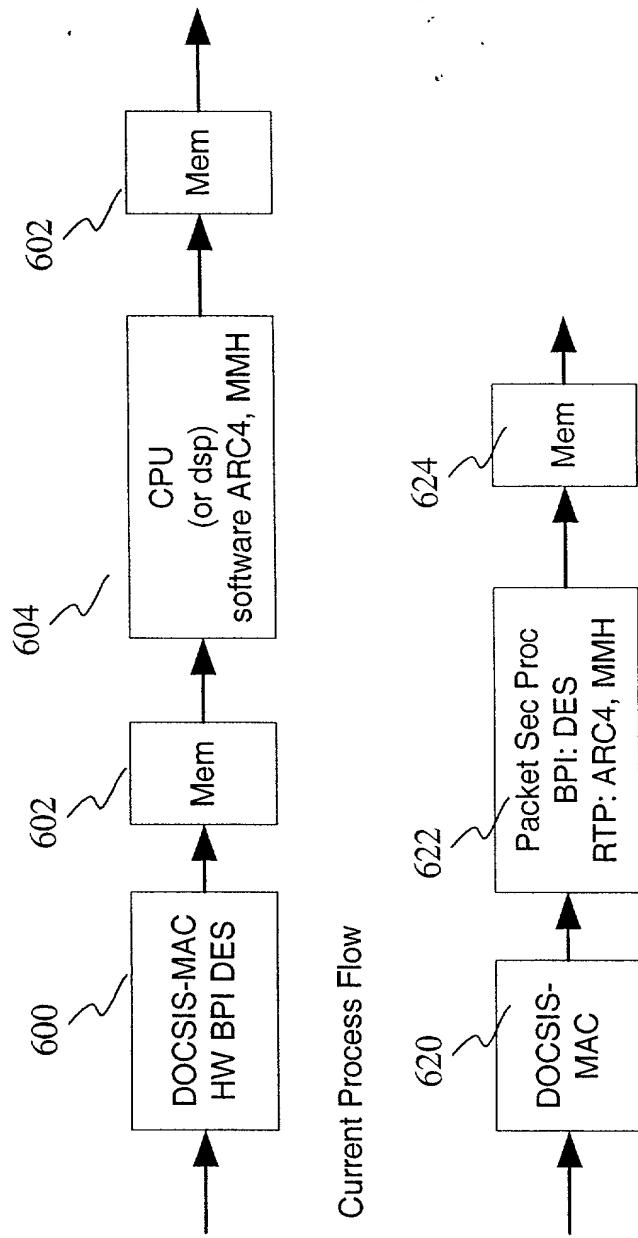


FIG. 10

Converged Security Process Flow

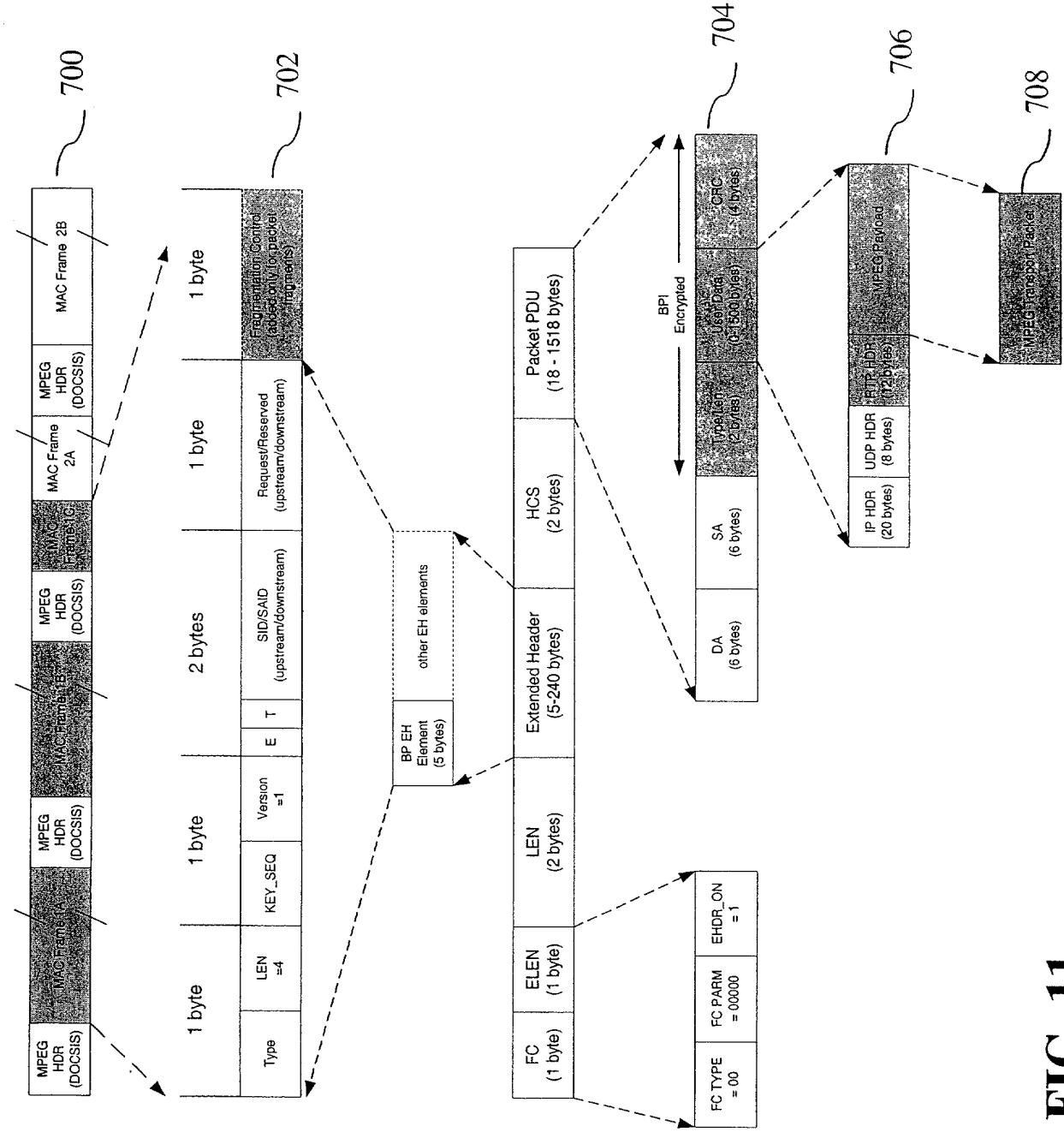
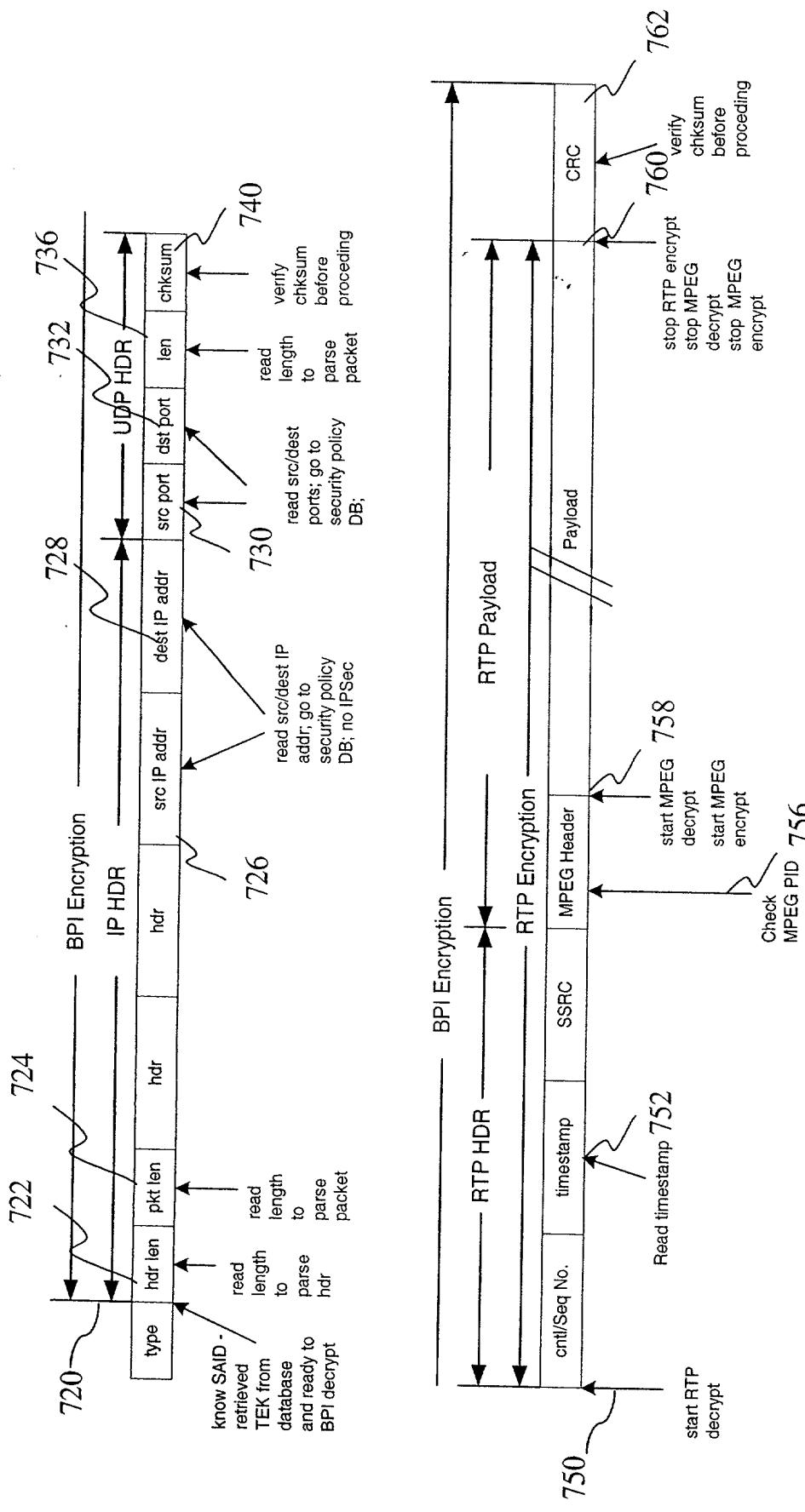


FIG. 11

FIG. 12



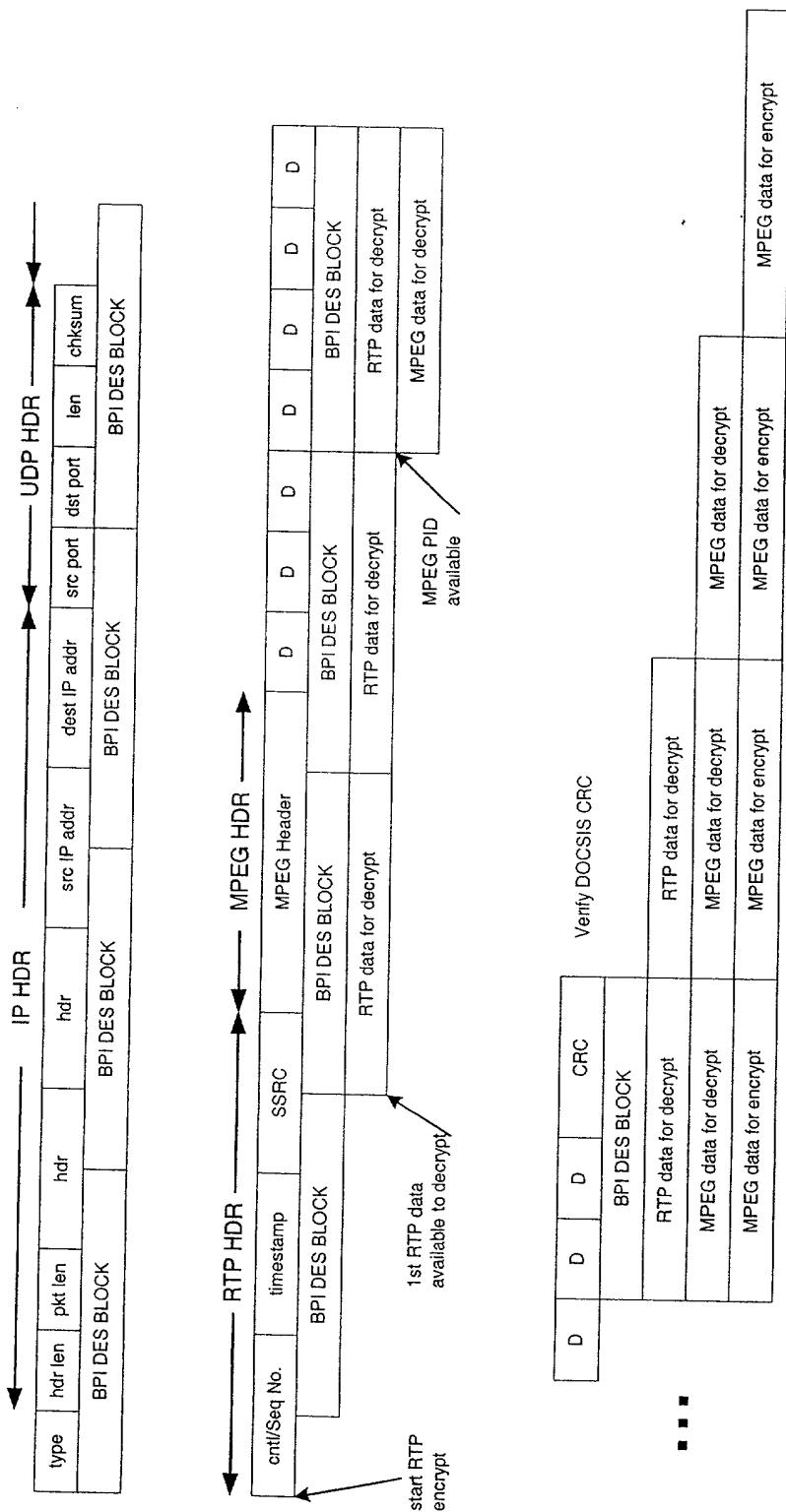


FIG. 13